IN THE CLAIMS

Following is a listing of the claims in the present application, marked to indicate changes proposed in the present response.

Claims 1 - 15 (Cancelled)

16. (Currently Amended) A high voltage semiconductor component, comprising:

a semiconductor body having a high voltage region and having an edge region of said high voltage region, a high voltage resistant structure at said edge region having at least one inner zone of a first conductivity type adjacent to a first surface of said semiconductor body;

a cell field including a plurality of individual high voltage components in said high voltage region, said high voltage individual components being connected in parallel and arranged in individual cells;

at least one floating guard ring of a second conductivity type arranged in said inner zone, said at least one floating guard ring surrounding said cell field; and

at least one inter-ring zone of said first conductivity type respectively arranged in said inner zone, said at least one inter-ring zone being arranged adjacent said at least one floating guard ring,

said at least one floating guard ring and said at least one inter-ring zone having respective doping levels such that a net doping level over a whole surface area of said edge region is approximately equal to zero, said at least one floating guard ring and said at least one inter-ring zone have ~~at least one of~~ conductivities and geometries set such that their free charge carriers are totally depleted when a blocking voltage is applied.

Claims 17, 18 and 19 (Cancelled)

20.(Previously Presented) The high voltage semiconductor component as claimed in claim 16, wherein said at least one floating guard ring has one of a U-shaped or V-shaped cross-section.

21.(Previously Presented) The high voltage semiconductor component as claimed in claim 16, further comprising:

at least one space charge zone stopper located at an outermost edge of said edge region of said semiconductor component.

22.(Previously Presented) The high voltage semiconductor component as claimed in claim 21, wherein said space charge zone stopper comprises a heavily doped region of said first conductivity type, said heavily doped region being arranged in said inner zone.

23.(Previously Presented) The high voltage semiconductor component as claimed in claim 21, wherein said space charge zone stopper comprises a damage implanted region being arranged in said inner zone.

24.(Previously Presented) The high voltage semiconductor component as claimed in claim 21, wherein said space charge zone stopper comprises an electrode connected to said inner zone, said electrode being one of metallic or containing polysilicon.

25.(Previously Presented) The high voltage semiconductor component as claimed in claim 16, further comprising:

at least one magnetoresistor located at an inner edge of said edge region of said semiconductor component.

26.(Previously Presented) The high voltage semiconductor component as claimed in claim 25, wherein at least one of said magnetoresistors is simultaneously a gate electrode of said semiconductor component.

27.(Previously Presented) The high voltage semiconductor component as claimed in claim 25, wherein at least an outermost of said magnetoresistors is nearly completely

enclosed by a cathode metallization in a direction of said first surface of said semiconductor component.

28.(Previously Presented) The high voltage semiconductor component as claimed in claim 27, wherein said cathode metallization is a metallization of a source electrode of said semiconductor component.

29.(Previously Presented) The high voltage semiconductor component as claimed in claim 16, wherein said at least one inter-ring zone in said edge region has a cross-section tapered to said first surface.

30.(Previously Presented) The high voltage semiconductor component as claimed in claim 16, wherein said individual high voltage components are one of vertical power transistors and IGBTs.

31.(Currently Amended) A semiconductor chip, comprising:

a substrate having a major surface;

a field of high voltage semiconductor components defining a high voltage portion in said substrate;

an edge structure at an edge of said high voltage portion, said edge structure separating said high voltage portion of said substrate from an edge of said major surface of said substrate, said edge structure including:

at least one inner zone of a first conductivity type defining a ring structure around said field of high voltage semiconductor components at said major surface;

at least one floating guard ring of a second conductivity type arranged in said at least one inner zone; and

at least one inter-ring zone of said first conductivity type arranged in said at least one inner zone, said at least one inter-ring zone being adjacent to said at least one floating guard ring,

at least one of said at least one inter-ring zone and said at least one floating guard ring being of a ~~at least one of a~~ conductivity and a geometry such that their free charge carriers are totally depleted when a blocking voltage is applied, said at least one inter-ring zone and said at least one floating guard ring having a net doping level over a whole surface area of said major surface of said at least one inner zone.

32.(Currently Amended) A semiconductor chip, comprising:

a substrate having a major surface;

a plurality of high voltage vertical MOSFET components in said substrate;

an edge structure at an edge of said plurality of high voltage vertical MOSFET components to separate said high voltage vertical MOSFET components from a remainder of said substrate, said edge structure including:

at least one inner zone of a first conductivity type defining a ring structure around said plurality of high voltage semiconductor components at said major surface;

at least one floating guard ring of a second conductivity type arranged in said at least one inner zone; and

an inter-ring zone of said first conductivity type arranged in said at least one inner zone, said inter-ring zone being adjacent to said at least one floating guard ring,

at least one of said inter-ring zone and said at least one floating guard ring being of ~~at least one of~~ a conductivity and a geometry such that their free charge carriers are totally depleted when a blocking voltage is applied, said at least one inter-ring zone and said at least one floating guard ring having respective doping levels such that a net doping level over said at least one inner zone is approximately equal to zero.

33. (Previously Presented) A high voltage semiconductor component as claimed in claim 16, wherein said at least one floating guard ring is a plurality of floating guard rings;

said at least one inter-ring zone is a plurality of inter-ring zones disposed between respective ones of said plurality of floating guard rings;

said plurality of floating guard rings being lightly doped at said second conductivity type;

said plurality of inter-ring zones being lightly doped at said first conductivity type.

34. (Previously Presented) A high voltage semiconductor component as claimed in claim 16, wherein said at least one floating guard ring is a plurality of floating guard rings;

said at least one inter-ring zone is a plurality of inter-ring zones disposed between respective ones of said plurality of floating guard rings;

said plurality of floating guard rings being doped at said second conductivity type;

said plurality of inter-ring zones being heavily doped at said first conductivity type.

35. (Previously Presented) A high voltage semiconductor component as claimed in claim 16, further comprising: a layer doped at said second conductivity type between respective ones of said floating guard rings and said inter-ring zones.

36. (Previously Presented) A high voltage semiconductor component as claimed in claim 16, further comprising: first and second layers between respective ones of said floating guard rings and said inter-ring zones, said first layer being doped at said first conductivity type and said second layer being doped at said second conductivity type.

37. (Previously Presented) A high voltage semiconductor component as claimed in claim 16, wherein said at least one floating guard ring is a plurality of floating guard rings;

said at least one inter-ring zone is a plurality of inter-ring zones disposed between respective ones of said plurality of floating guard rings;

said plurality of floating guard rings extending into said inner zone of said semiconductor body in substantially parallel columnar cross sections disposed at a regular spacing from one another.

38. (Previously Presented) A high voltage semiconductor component as claimed in claim 37, wherein each of said plurality of floating guard rings extend to a same depth into said semiconductor body.

39. (Withdrawn) A high voltage semiconductor component as claimed in claim 37, wherein said plurality of floating guard rings extend to mutually different depths into said semiconductor body.

40. (Withdrawn) A high voltage semiconductor component as claimed in claim 39, wherein said plurality of floating guard rings have mutually different flank angles of trench walls of said guard rings.

41. (Withdrawn) A high voltage semiconductor component as claimed in claim 16, wherein said at least one floating guard ring is a plurality of floating guard rings;

said at least one inter-ring zone is a plurality of inter-ring zones disposed between respective ones of said plurality of floating guard rings;

said plurality of floating guard rings extending into said inner zone of said semiconductor body at a mutually different spacings from one another.

42. (Withdrawn) A high voltage semiconductor component as claimed in claim 41, wherein said mutually different spacings increase from said high voltage region to said edge region.

43. (Withdrawn) A high voltage semiconductor component as claimed in claim 16, wherein said at least one floating guard ring is a plurality of floating guard rings;

said at least one inter-ring zone is a plurality of inter-ring zones disposed between respective ones of said plurality of floating guard rings;

said plurality of floating guard rings have mutually different thicknesses in a direction perpendicular to said first surface.

44. (Withdrawn) A high voltage semiconductor component as claimed in claim 43, wherein said mutually different thicknesses decrease from said high voltage region to said edge region.

45. (Previously Presented) A semiconductor chip as claimed in claim 31, wherein said at least one floating guard ring is a plurality of floating guard rings;

said at least one inter-ring zone is a plurality of inter-ring zones disposed between respective ones of said plurality of floating guard rings;

said plurality of floating guard rings being lightly doped at said second conductivity type;

said plurality of inter-ring zones being lightly doped at said first conductivity type.

46. (Previously Presented) A semiconductor chip as claimed in claim 31, wherein said at least one floating guard ring is a plurality of floating guard rings;

said at least one inter-ring zone is a plurality of inter-ring zones disposed between respective ones of said plurality of floating guard rings;

said plurality of floating guard rings being doped at said second conductivity type;

said plurality of inter-ring zones being heavily doped at said first conductivity type.

47. (Previously Presented) A semiconductor chip as claimed in claim 31, further comprising: a layer doped at said second conductivity type between respective ones of said floating guard rings and said inter-ring zones.

48. (Previously Presented) A semiconductor chip as claimed in claim 31, further comprising: first and second layers between respective ones of said floating guard rings and

said inter-ring zones, said first layer being doped at said first conductivity type and said second layer being doped at said second conductivity type.

49. (Withdrawn) A semiconductor chip as claimed in claim 31, wherein said at least one floating guard ring is a plurality of floating guard rings;

said at least one inter-ring zone is a plurality of inter-ring zones disposed between respective ones of said plurality of floating guard rings;

said plurality of floating guard rings extending into said inner zone of said semiconductor body in substantially parallel columnar cross sections disposed at a regular spacing from one another.

50. (Withdrawn) A semiconductor chip as claimed in claim 49, wherein each of said plurality of floating guard rings extend to a same depth into said semiconductor body.

51. (Withdrawn) A semiconductor chip as claimed in claim 49, wherein said plurality of floating guard rings extend to mutually different depths into said semiconductor body.

52. (Withdrawn) A semiconductor chip as claimed in claim 51, wherein said plurality of floating guard rings have mutually different flank angles of trench walls of said guard rings.

53. (Withdrawn) A semiconductor chip as claimed in claim 31, wherein said at least one floating guard ring is a plurality of floating guard rings;

said at least one inter-ring zone is a plurality of inter-ring zones disposed between respective ones of said plurality of floating guard rings;

said plurality of floating guard rings extending into said inner zone of said semiconductor body at a mutually different spacings from one another.

54. (Withdrawn) A semiconductor chip as claimed in claim 53, wherein said mutually different spacings increase from said high voltage region to said edge region.

55. (Withdrawn) A semiconductor chip as claimed in claim 31, wherein said at least one floating guard ring is a plurality of floating guard rings;

said at least one inter-ring zone is a plurality of inter-ring zones disposed between respective ones of said plurality of floating guard rings;

said plurality of floating guard rings have mutually different thicknesses in a direction perpendicular to said first surface.

56. (Withdrawn) A semiconductor chip as claimed in claim 55, wherein said mutually different thicknesses decrease from said high voltage region to said edge region.